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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/623,732	07/22/2003	Kyoichi Suguro	04329.2344-02	6071

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EXAMINER	
DOAN, THERESA T	

ART UNIT	PAPER NUMBER
2814	

MAIL DATE	DELIVERY MODE
10/29/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/623,732	SUGURO ET AL.	
	Examiner	Art Unit	
	Theresa T. Doan	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 September 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *38-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *38-41* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/609107.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The RCE and the amendment filed on 09/11/07 have been acknowledged and entered. By this amendment, claims 1-37 are canceled and claims 38-41 are pending in the application.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 38-41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iwata et al. (6,426,532).

Regarding claims 38-39, Iwata (Fig. 6A) discloses a semiconductor device comprising: a substrate 200 having a semiconductor layer (212,202,203) and a trench (corresponding to the 201 device isolation region), the semiconductor layer being an epitaxial layer (column 23, lines 11-13), the trench partitioning the semiconductor layer into a plurality of regions; an element isolating insulating film 201 provided in the trench for partitioning the semiconductor layer into a plurality of element regions, the element isolating insulating film 201 having a top surface projecting upward above a top surface of the semiconductor layer 202, wherein the element isolation insulating film 201 is an oxide film; and a MOS type element formed within a corresponding one of the element

regions and having a gate insulating film 205 and a gate electrode 206 on the gate insulating film 205, wherein: a difference in height from the substrate between a top surface position of the element isolating insulating film 201 and the top surface position of the element isolating insulating film 201 is not higher than a top surface position of the gate electrode 206, the element isolating insulating film 201 and each of the element regions make an interface which is substantially perpendicular to the top surface of the semiconductor layer 202, the element isolating insulating film 201 further having a side surface projecting above the top surface of the semiconductor layer 202 wherein the side surface is substantially perpendicular to the top surface of the semiconductor layer 202 such that a corner portion having a substantially right angle is formed by the top surface of the semiconductor layer 202 and the side surface of the element isolating insulating film projecting above the top surface, the gate electrode 206 is formed on the gate insulating film 205, the gate insulating film 205 being formed on the top surface of the semiconductor layer 202 in each of the element regions which is not covered with the element isolating insulating film 201, and the gate electrode 206 is formed on the gate insulating film 205 (Fig. 6A).

Iwata (Fig. 6A) discloses a difference in height from the substrate between a top surface position of the element isolating insulating film 201 and a top surface position of the semiconductor layer 202 but does not disclose the difference in height from the substrate between a top surface position of the element isolating insulating film 201 and a top surface position of the semiconductor layer 202 is at least three times as large as the thickness of the gate insulating film 205 or at least 10nm. It has been held that

where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation. *In re Aller*, 220 F. 2d 454, 105 USPQ 233, 235 (CCPA 1955). Therefore, it would have been obvious to modify the device of Iwata by forming the difference in height from the substrate between a top surface position of the element isolating insulating film 201 and a top surface position of the semiconductor layer 202 is at least three times as large as the thickness of the gate insulating film 205 or at least 10nm because the difference in height as discussed above can be varied depending upon the size desired for the semiconductor device. Furthermore, nowhere in the present application indicates the criticality of having the difference in height from the substrate between a top surface position of the element isolating insulating film and a top surface position of the semiconductor layer is at least three times as large as the thickness of the gate insulating film or at least 10nm.

Regarding claims 40-41, Iwata (Fig. 6A) discloses the gate electrode 206 contacts the side surface of the element isolating insulating 201 in vertical cross-section perpendicular to a gate length direction of the MOS type element.

Response to Amendment

Applicant's arguments with respect to claims 38-41 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Theresa T. Doan whose telephone number is (571) 272-1704. The examiner can normally be reached on Monday, Tuesday and Thursday from 7:00AM - 3:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, WAEL FAHMY can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Theresa T. Doan/
Primary Examiner, Art Unit 2814